IN THE CLAIMS

Claims 1-27 have previously been cancelled. Please amend the following claims which are pending in the present application:

28. (Previously presented) A semiconductor transistor, comprising:

a layer having source and drain recesses formed therein with a channel between the source and drain recesses, and being made of a semiconductor material having a first lattice with a first structure and a first spacing;

a source and a drain formed in the source and drain recesses respectively, at least one of the source and the drain being made of a film material which:

(a) includes a p-dopant; and

(b) is formed epitaxially on the semiconductor material so as to have a second lattice having a second structure which is the same as the first structure, the second lattice having a second spacing which is larger than the first spacing, so that a compressive stress is created between the source and the drain in the channel;

a gate dielectric layer on the channel; and

a conductive gate electrode on the gate dielectric layer.

29. (Previously presented) The semiconductor transistor of claim 28, wherein the second material includes the semiconductor material and an additive, the difference between the first spacing and the second spacing being due to the additive.

30. (Previously presented) The semiconductor transistor of claim 29, wherein the additive is germanium.

31. (Previously presented) The semiconductor transistor of claim 29, further comprising:

tip regions formed between the source and the drain with the channel between the tip regions, the tip regions being formed by implanting of dopants and excluding the additive.

32. (Previously presented) The semiconductor transistor of claim 31, wherein the dopants of the tip regions are p-dopants.

33. (Previously presented) A semiconductor transistor comprising:

a layer having source and drain recesses formed therein with a channel between the source and drain recesses, and being made of a semiconductor material having a first lattice with a first structure and a first spacing;

a source and a drain formed in the source and drain recesses respectively, at least one of the source and the drain being made of a film material which:

(a) includes an n-dopant; and

(b) is formed epitaxially on the semiconductor material so as to have a second lattice having a second structure which is the same as the first structure, the second lattice having a second spacing which is smaller than the first spacing, so that a tensile

stress is created between the source and the drain in the channel;

a gate dielectric layer on the channel; and

a conductive gate electrode on the gate dielectric layer.

34. (Previously presented) The semiconductor transistor of claim 33, wherein the second material includes the semiconductor material and an additive, the difference between the first spacing and the second spacing being due to the additive.

35. (Previously presented) The semiconductor transistor of claim 34, wherein the additive is carbon.

36. (Previously presented) The semiconductor transistor of claim 34, further comprising:

tip regions formed between the source and the drain with the channel between the tip regions, the tip regions being formed by implanting of dopants and excluding the additive.

37. (Previously presented) The semiconductor transistor of claim 36, wherein the dopants of the tip regions are n-dopants.

38. (Currently amended) A semiconductor transistor comprising:

a layer having source and drain recesses formed therein with a channel between

the source and drain recesses, and being made of a semiconductor material having a first lattice with a first structure and a first spacing and at least the channel, the semiconductor material including an n-dopant;

a source and a drain formed in the source and drain recesses respectively, at least one of the source and the drain being made of a film material which is formed epitaxially on the semiconductor material so as to have a second lattice having a second structure which is the same as the first structure, the second lattice having a second spacing which is larger than the first spacing, so that a compressive stress is created between the source and the drain in the channel;

a gate dielectric layer on the channel; and

a conductive gate electrode on the gate dielectric layer.

39. (Currently amended) A semiconductor transistor comprising:

a layer having source and drain recesses formed therein with a channel between the source and drain recesses, and being made of a semiconductor material having a first lattice with a first structure and a first spacing and at least the channel, the semiconductor material including a p-dopant;

a source and a drain formed in the source and drain recesses respectively, at least one of the source and the drain being made of a film material which is formed epitaxially on the semiconductor material so as to have a second lattice having a second structure which is the same as the first structure, the second lattice having a second spacing which is smaller than the first spacing, so that a tensile stress is created

between the source and the drain in the channel;

a gate dielectric layer on the channel; and

a conductive gate electrode on the gate dielectric layer.